AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A system, comprising:

a memory configured to store data; and

a device coupled to the memory, wherein the device includes a random number generator, wherein the random number generator includes:

an entropy register configured to receive bits over a plurality of data lines, wherein each of the plurality of data lines couples an individual entry in the entropy register with an ~~a corresponding~~ entry in ~~another register~~ a corresponding one of a plurality of performance registers.

2. (Original) The system of claim 1, wherein the random number generator further includes:

an entropy control unit configured to provide a value from the entropy register in response to a request for a random number.

3. (Canceled)

4. (Currently Amended) The system of claim [[3]] 1, wherein the corresponding entry in the one of the plurality of performance registers corresponds to the least significant bit entry in each of the plurality of performance registers.

5. (Canceled)

6. (Original) The system of claim 1, wherein the device includes a processor.

7. (Original) The system of claim 1, further comprising:

a bridge coupled between the memory and the device.

8. (Original) The system of claim 1, wherein the device is configured to cause data to be stored in the memory.

9. (Currently Amended) A device, comprising:

a random number generator coupled to receive signals from a plurality of bit lines, wherein the random number generator includes:

an entropy register configured to receive bits over the plurality of data lines, wherein each of the plurality of data lines couples an individual entry in the entropy register with an ~~a corresponding~~ entry in ~~another register~~ a corresponding one of a plurality of performance registers.

10. (Original) The device of claim 9, wherein the random number generator further includes:

an entropy control unit configured to provide a value from the entropy register in response to a request for a random number.

11-12. (Canceled)

13. (Currently Amended) The device of claim [[12]] 1, wherein the corresponding entry in the one of the plurality of performance registers corresponds to the least significant bit entry in each of the plurality of performance registers.

14. (Canceled)

15. (Original) The device of claim 9, wherein the device includes a processor.

16. (Currently Amended) A random number generator, comprising:

a plurality of data lines, each data line being coupled to a corresponding one of a plurality of performance registers; and

an entropy register configured to receive bits from the plurality of performance registers over [[a]] the plurality of data lines ~~that each couple to an individual entry in the entropy register~~.

17. (Original) The random number generator of claim 16, further comprising:

an entropy control unit configured to provide a value from the entropy register in response to a request for a random number.

18-20. (Canceled)

21. (Currently Amended) The random number generator of claim 16 [[20]], wherein the corresponding entry in the one of the plurality of performance registers corresponds to the least significant bit entry in each of the plurality of performance registers.

22. (Currently Amended) A method of generating a random number, the method comprising:

providing a first plurality of bit entries in an entropy register; and

transmitting a bit value from each of a plurality of performance registers to one of the first plurality of bit entries in the entropy register.

23. (Original) The method of claim 22, further comprising:

providing the bit values from each of the first plurality of bit entries in the entropy register.

24. (Original) The method of claim 23, further comprising:

receiving a request for a random number;

wherein providing the bit values from each of the first plurality of bit entries in the entropy register comprises providing the bit values from each of the first plurality of bit entries in the entropy register in response to receiving the request for the random number.

25. (Canceled)

26. (Original) The method of claim 24, further comprising:

prior to providing the bit values from each of the first plurality of bit entries in the entropy register, providing a control signal to the entropy register; and

reading the bit values from each of the first plurality of bit entries in the entropy register.

27-30. (Canceled)

31. (Currently Amended) A method for generating a random number, the method comprising:

step for providing a first plurality of bit entries; and

step for transmitting a bit value from each of a plurality of performance registers to one of the first plurality of bit entries.

32. (Original) The method of claim 31, further comprising:

step for providing the bit values from each of the first plurality of bit entries.

33. (Original) The method of claim 32, further comprising:

step for receiving a request for a random number;

wherein the step for providing the bit values from each of the first plurality of bit entries comprises step for providing the bit values from each of the first plurality of bit entries in response to the step for receiving the request for the random number.

34. (Original) The method of claim 33, wherein the step for receiving the request for the random number includes step for receiving a length in bits for the random number, and wherein the length in bits for the random number is less than or equal to a number of bit entries in the first plurality of bit entries.

35. (Original) The method of claim 33, further comprising:

prior to the step for providing the bit values from each of the first plurality of bit entries,

step for controlling the first plurality of bit entries; and

step for reading the bit values from each of the first plurality of bit entries.

36. (Currently Amended) A computer readable program storage device encoded with instructions that, when executed by a computer, performs a method of generating a random number, the method comprising:

providing a first plurality of bit entries to an entropy register; and

transmitting a bit value from each of a plurality of performance registers to one of the first plurality of bit entries in the entropy register.

37. (Original) The computer readable program storage device of claim 36, the method further comprising:

providing the bit values from each of the first plurality of bit entries in the entropy register.

38. (Original) The computer readable program storage device of claim 36, the method further comprising:

receiving a request for a random number;

wherein providing the bit values from each of the first plurality of bit entries in the entropy register comprises providing the bit values from each of the first plurality of bit entries in the entropy register in response to receiving the request for the random number.

39. (Original) The computer readable program storage device of claim 38, wherein receiving the request for the random number includes receiving a length in bits for the random number,

and wherein the length in bits for the random number is less than or equal to a number of bit entries in the first plurality of bit entries.

40. (Original) The computer readable program storage device of claim 38, further comprising:

prior to providing the bit values from each of the first plurality of bit entries in the entropy register,

providing a control signal to the entropy register; and

reading the bit values from each of the first plurality of bit entries in the entropy register.